

AMENDMENT TO THE DRAWINGS

Please find enclosed replacement sheets for Figs. 17 and 18 with proposed corrections thereon for the approval of the Examiner.

REMARKS/ARGUMENTS

Applicant responds herein to the Office Action dated January 10, 2006. A Petition for Extension of Time (one month) and the fee therefor are enclosed.

The drawings were objected to in paragraphs 3 and 4 of the Office Action. Reconsideration of the objection is respectfully requested.

In response to the objections in paragraph 3 of the Office Action, replacement sheets for Figs. 17 and 18 are enclosed herewith for the approval of the Examiner correcting reference character 10 in Figs. 17 and 18 to read 10' and 10" respectively, in accordance with the suggestion of the Examiner.

With respect to the objection to the drawings in paragraph 4 of the Office Action, the specification has been amended in accordance with the suggestion of the Examiner.

The title of the invention has been objected to as not descriptive. Reconsideration of the objection is respectfully requested. The title has been amended in accordance with the suggestion of the Examiner.

The abstract of the disclosure has been objected to. Reconsideration of the objection is respectfully requested. The abstract of the disclosure has been amended in accordance with the suggestions of the Examiner.

The disclosure was objected to for various informalities. Reconsideration of the objection is respectfully requested.

The errors have been corrected in accordance with the suggestion of the Examiner, except that "(Correct)", paragraph [00218], line 1, has not been changed as it is respectfully submitted that this is not an error.

Claims 1-6 and 9-12 were objected to. Reconsideration of the objection is respectfully requested.

The errors in claim 1, paragraph 7, line 3 and claim 3, paragraph 5, line 6, have been corrected. With respect to the errors in claims 4 and 5, paragraph 1, line 3, those portions of paragraph 1 have been deleted, and, therefore, the objections have been overcome. The error in claim 9, paragraph 2, line 1, has been corrected. With regard to the objection to claims 2-3, 6, and

10-12 because of their dependence on claim 1, it is respectfully submitted that claims 6 and 10-12 are in fact dependent on claim 3. Insofar as claims 2-3 are concerned, Applicants do not understand the ground for the objection based on the dependence of claims 2-3 on claim 1 and, therefore, do not know what remedial action to take. Applicants respectfully request the Examiner to either explain the reason for the objections so that Applicants can properly amend the claim to overcome it or withdraw the objection.

With respect to paragraph 10 of the Office Action, the changes to the claims suggested by the Examiner have been made.

Claims 1 and 3-4 were rejected under 35 U.S.C. §102(e) as being anticipated by Nakai, et. al. (US 2003/0061536). Reconsideration of the rejection is respectfully requested.

Independent claim 1 was amended to provide, in part, for,

“[a] semiconductor integrated circuit device having a dynamic RAM, said dynamic RAM comprising a memory array, a RAM control section, an ECC-codec circuit, and an ECC controller, said RAM control section comprising a command decoding section responsive to an external command from the outside of said dynamic RAM for decoding the external command and a super self-refresh control circuit, said super self-refresh control circuit being contained within said RAM control section, wherein:

...said ECC controller comprises a command generating section and an address generating section, said address generating section being contained within said ECC controller;...”.

Antecedent basis for the amendment to independent claim 1 is found in the specification, for example, on p.10, para.[0077], lines 1-2, p.12, para.[0085], lines 1-5, and p.15, para.[0094], lines 1-2, and in the drawings in, for example, Figs. 1 and 3.

In contrast, the Examiner alleges that the RAM control section of independent claim 1 is equivalent to element 21 of Fig. 1 in Nakai (Office Action, p.5, ¶ 13, lines 4-5), the super self-refresh control circuit of independent claim 1 is equivalent to element 22 of Fig. 1 of Nakai (Office Action, p.5, ¶ 13, lines 9-10), the address generating section of independent claim 1 is equivalent to element 9 of Fig. 1 in Nakai (Office Action, p.6, line 5), and the ECC controller of independent claim 1 is equivalent to element 23 of Fig. 1 in Nakai (Office Action, p.6, line 4). It is clear from Fig. 1 in Nakai that element 22 is not contained within element 21 and that element 9 is not contained within element 23, contrary to amended independent claim 1.

Since claims 3-4 are directly or indirectly dependent upon independent claim 1, they are allowable over Nakai for the same reasons recited above with respect to the allowability of independent claim 1 of Nakai.

Claims 2 and 5 were rejected under 35 U.S.C. §103(a) as being unpatentable over Nakai as applied to claims 1 and 3-4, and further in view of the Attaway, et. al. (6,829,677). Reconsideration of the rejection is respectfully requested.

Since claims 2 and 5 are directly or indirectly dependent upon independent claim 1, they are allowable over Nakai for the same reasons recited above with respect to the allowability of independent claim 1 over Nakai.

With respect to Attaway et al., it does not disclose, teach or suggest a super self-refresh control circuit being contained within a RAM control section and an address generating section contained within an ECC controller, as claimed in independent claim 1, and therefore, in dependent claims 2 and 5.

Claim 6 was rejected under 35 U.S.C. §103(a) as being anticipated by Nakai as applied to claims 1 and 3-4, and further in view of Sawhney (US 2002/0133663). Reconsideration of the rejection is respectfully requested.

Since claim 6 is indirectly dependent upon independent claim 1, it is allowable over Nakai for the same reasons recited above with respect to the allowability of independent claim 1 over Nakai.

With respect to Sawhney, it does not disclose, teach or suggest a super self-refresh control circuit contained within a RAM control section and an address generating section contained within an ECC controller, as claimed in independent claim 1, and therefore, in dependent claim 6.

Claims 7 and 9-11 were rejected under U.S.C. §103(a) as being anticipated by Nakai as applied to claims 1 and 3-4, and further in view of Dell (5,450,422). Reconsideration of the rejection is respectfully requested.

Independent claim 7 has been amended to provide, in part, for,

“[a] semiconductor integrated circuit device having a dynamic RAM, said dynamic RAM comprising a memory array, a RAM control section, an error correction circuit, and a BIST (built-in-self-test) controller,...wherein:...

said BIST controller comprises a command generating section and an address generating section, said address generating section being contained within said BIST controller;...”.

Antecedent basis for the amendment to independent claim 7 is found in the specification, for example, on p. 31, para.[0182], lines 1-3, and para.[0183], lines 1-3, and in the drawings, for example, in Fig. 12.

In contrast, the Examiner alleges that the address generating section of independent claim 7 is equivalent to element 9 of Fig. 1 in Nakai (Office Action, p.13, line 9), and that the BIST controller of independent claim 7 is equivalent to element 23 of Fig. 1 in Nakai (Office Action, p.13, line 8). As indicated before with reference to independent claim 1, Fig. 1 of Nakai clearly shows that element 9 is not contained within element 23, contrary to amended independent claim 7.

Since claim 9 is directly dependent upon independent claim 7, it is allowable over Nakai for the same reasons recited above with respect to the allowability of independent claim 7 over Nakai.

Since claims 10-11 are indirectly dependent upon independent claim 1, they are allowable over Nakai for the same reasons recited above with respect to the allowability of independent claim 1 over Nakai

With respect to Dell, it does not disclose, teach, or suggest an address generating section contained within a BIST controller, as claimed in independent claim 7, and, therefore, in dependent claim 9. It also does not disclose, teach, or suggest a super self-refresh control circuit contained within a RAM control section and an address generating section contained within an ECC controller, as claimed in independent claim 1, and, therefore, in dependent claims 10-11.

Claim 8 was rejected under 35 U.S.C. §103(a) as being anticipated by Nakai, in view of Dell as applied to claims 7 and 9-11, and further in view of Attaway. Reconsideration of the rejection is respectfully requested.

Since claim 8 is directly dependent upon independent claim 7, it is allowable over Nakai for the same reasons recited above with respect to the allowability of independent claim 7 over Nakai.

With respect to Dell, claim 8 is allowable over Dell for the same reasons recited above with respect to the allowability of dependent claim 9 over Dell.

With respect to Attaway, Attaway does not disclose, teach, or suggest an address generating section contained within a BIST controller, as claimed in independent claim 7, and, therefore, in dependent claim 8.

Claim 12 was rejected under 35 U.S.C. §103(a) as being anticipated by Nakai and further in view of Saiki et al., JP 362078920. Reconsideration of the rejection is respectfully requested.

Since claim 12 is indirectly dependent upon independent claim 1, it is allowable over Nakai for the same reasons recited above with respect to the allowability of independent claim 1 over Nakai.

With respect to Saiki, Saiki does not disclose, teach, or suggest a super self-refresh control circuit contained within a RAM control section and an address generating section contained within an ECC controller, as claimed in independent claim 1, and, therefore, in dependent claim 12.

In view of the foregoing amendments and remarks, allowance of claims 1-12 is respectfully requested.

Accordingly, the Examiner is respectfully requested to reconsider the application, allow the claims as amended and pass this case to issue.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on May 1, 2006

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Name of applicant, assignee or
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Signature
May 1, 2006

Date of Signature

Respectfully submitted,

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